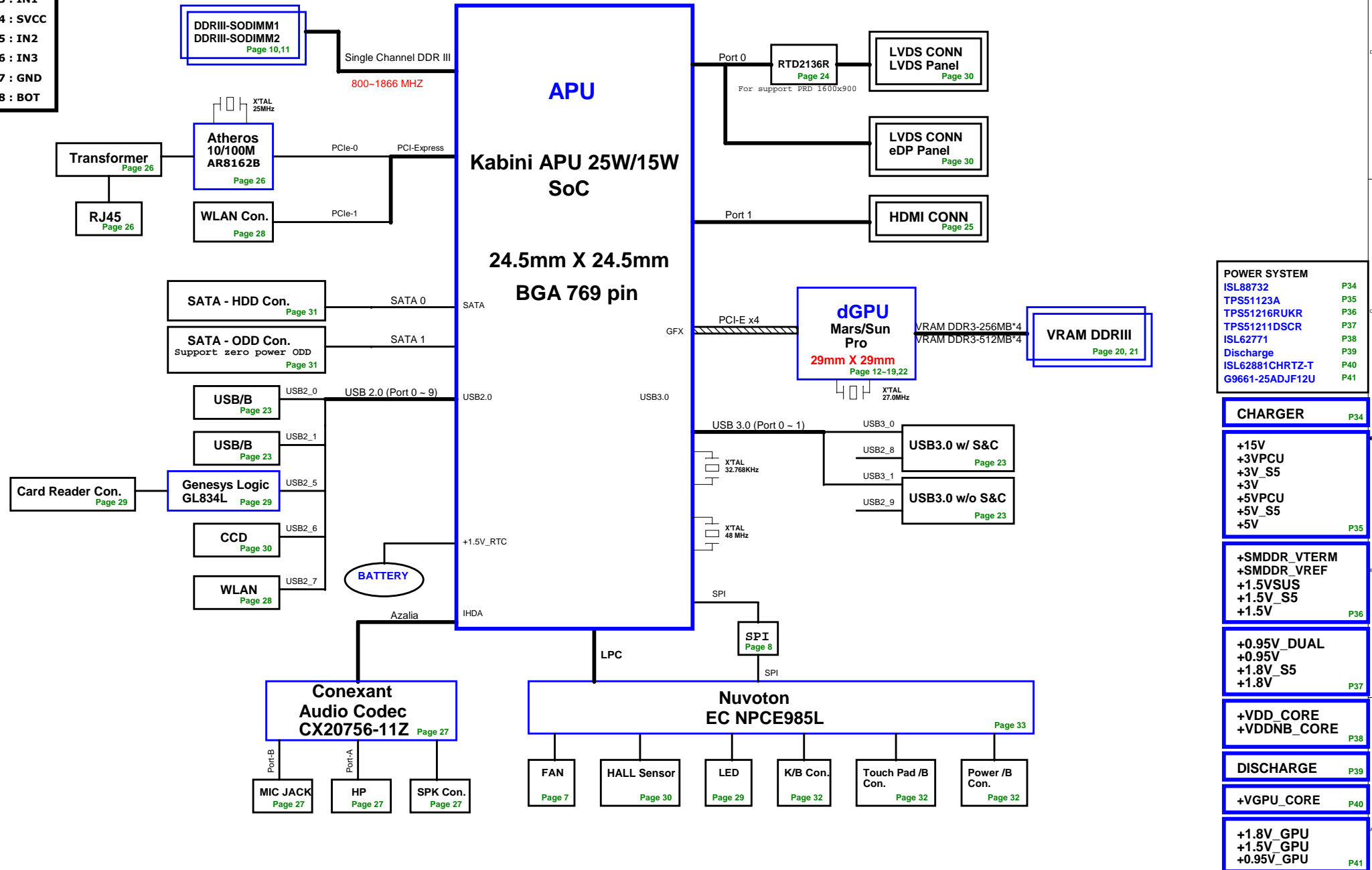


## PCB STACK UP

LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : SVCC  
 LAYER 5 : IN2  
 LAYER 6 : IN3  
 LAYER 7 : GND  
 LAYER 8 : BOT

## BD9 FT3 Kabini Block Diagram



**POWER SYSTEM**

- ISL88732 P34
- TPS51123A P35
- TPS51216RUKR P36
- TPS51211DSCR P37
- ISL62771 P38
- Discharge P39
- ISL62881CHRTZ-T P40
- G9661-25ADJF12U P41

## CHARGER P34

+15V  
 +3VPCU  
 +3V\_S5  
 +3V  
 +5VPCU  
 +5V\_S5  
 +5V P35

+SMDDR\_VTERM  
 +SMDDR\_VREF  
 +1.5VSUS  
 +1.5V\_S5  
 +1.5V P36

+0.95V\_DUAL  
 +0.95V  
 +1.8V\_S5  
 +1.8V P37

+VDD\_CORE  
 +VDDNB\_CORE P38

## DISCHARGE P39

+VGPU\_CORE P40

+1.8V\_GPU  
 +1.5V\_GPU  
 +0.95V\_GPU P41








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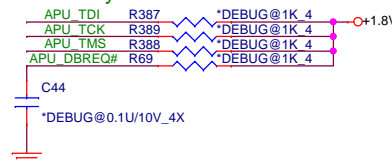
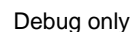
PROJECT : BD9

Table of Contents

PAGE	DESCRIPTION	BOI-FUNCTION
1	Schematic Block Diagram	
2	Power Stage	
3 - 8	Processor	CPU
9	Straps	CPU
10	SO-DIMM 1	DDR
11	SO-DIMM 2	DDR
12 - 19	Mars/Sun Pro(M2)	VGA
20 - 21	VRAM - DDR3	VGA
22	PX5	VGA
23	USB	U3B/USB
24	eDP to LVDS(RTD2136R)	LDS
25	HDMI/Touch Screen	HDM/TSN
26	LAN(1AR8162B)	LAN
27	Codec (CX20756-11Z)	ADO
28	MINI CARD (WLAN)	MNW
29	CARD READER(GL834L)/LED	MMC/LED
30	LDS/CRT/CCD	LDS/CRT/CCD
31	HDD/ODD	HDD/ODD
32	KB/TouchPad	KBC/TPD
33	EC 985L	KBC
34	Charger (ISL88731CHRTZ-T)	CHR
35	System 5V/3V	PWM
36	DDR 1.5V	PWM
37	+0.95V_DUAL	PWM
38	+VCC_CORE	PWM
39	Discharge	PWM
40	GPU_CORE	PWM
41	+0.95V_GPU/+1.8V_GPU/+1.5V_GPU/+3V_GPU	PWM

GND PLANE	PAGE
 GND_SIGNAL	
 8769GND	
	
 GND	ALL
 ADOGND	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+1.5V		S0~S5
+3V	+3.3V	MAIND	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3VPCU	+3.3V	AC/DC Insert enable	S0~S5
+5V	+5V	MAIND	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+WIMAX_P	+3.3V	IOAC_EN	S0
+1.5VSUS	+1.5V	SUSON	S0~S3
+1.5V	+1.5V	MAIND	S0
+1.8V_S5	+1.8V	PE_PWRGD ^ PE_GPIO1	S0~S5
+0.95V_DUAL	+0.95V	+0.95V_DUAL_EN	S0~S5
+0.95V	+0.95V	MAIND	S0
+VDD_CORE	~	VRON	S0
+VDDNB_CORE	~	VRON	S0
+VGPU_CORE		GPU_MAINON ^ PE_GPIO1	S0
+1.8V_GPU	+1.8V	GPU_MAIND	S0
+0.95V_GPU	+0.95V	GPU_MAINON ^ PE_GPIO1	S0
+3V_GPU	+3.3V	GPU_MAIND	S0
+1.5V_GPU	+1.5V	GPU_MAIND	S0

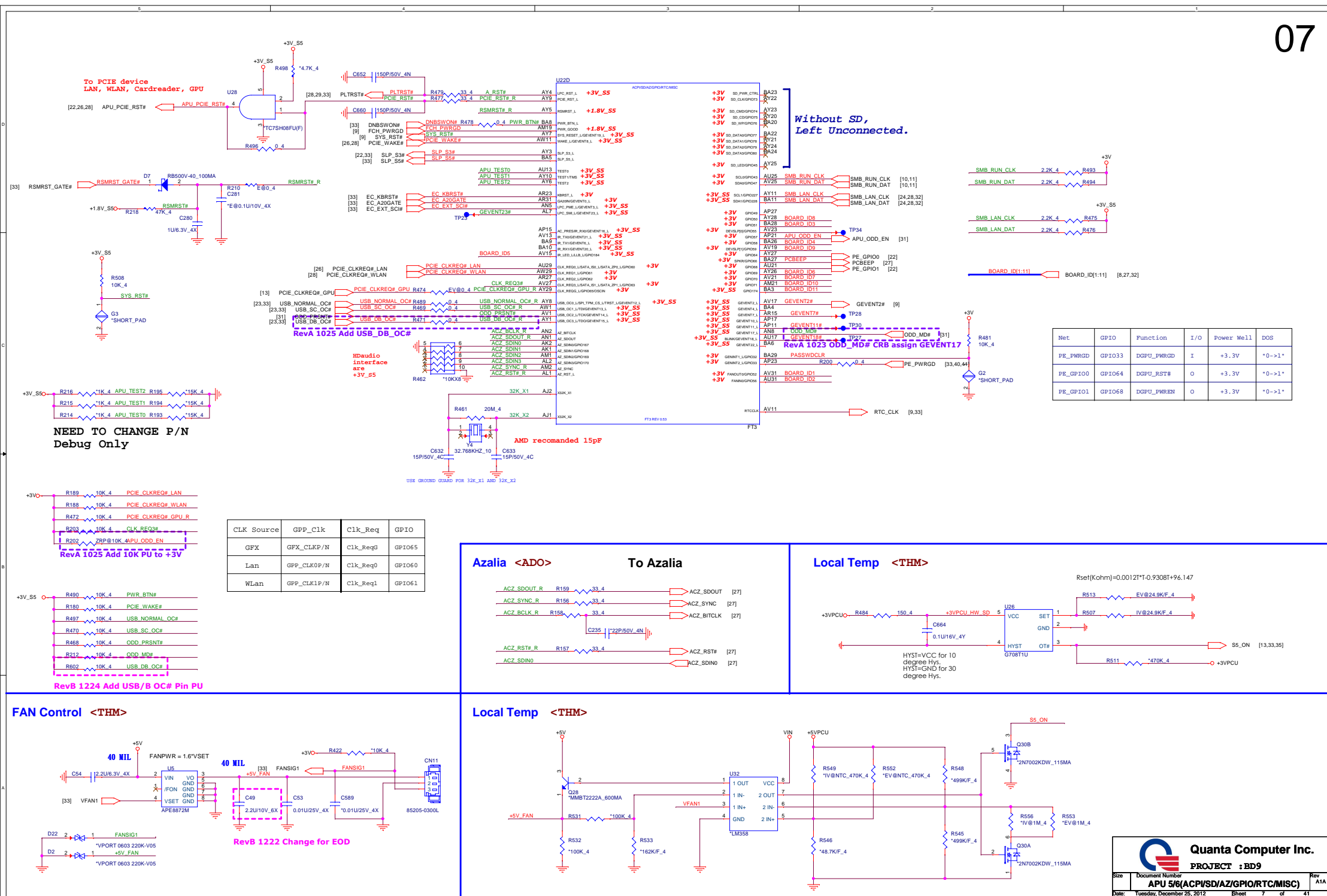


**RevB 1221 Add 0 ohm for debug**











SATA HDD

SATA ODD

Reference GND  
Do not change layer  
and cross plane

RevB 1222 Change cap value for vendor suggestion

For EMI

## BOARD ID SETTING

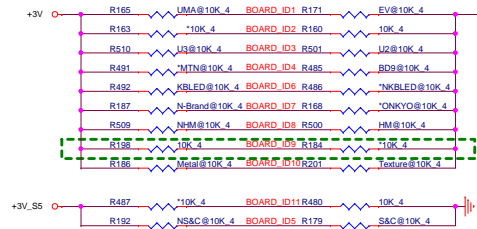
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12	ID13
UMA SKU		H											
PX SKU		L											
VRAM 1GHZ			H										
VRAM 900M			L										
USB3.0				H									
USB2.0													
14" MTN													
17" BD9													
W/O S&C													
W S&C													
N-METAL (W/O KBLED)													
METAL (W/ KBLED)													
N-Brand													
Brand (ONKYO)													
W/O HDMI													
W HDMI													
N-Brand													
Brand (Harman/Kardon)													
Metal/IMR													
TEXTURE													
RSVD													
RSVD													

RevB 1221 Modify Board ID

RevC 0130 Change Board ID setting

Reserve PD

[7.27.32] BOARD\_ID[1:11] BOARD\_ID[1:11]



RevC 0130 Change Board ID 9 for Harman-Kardon Stuff R198, Remove R184

HUB1

HUB2

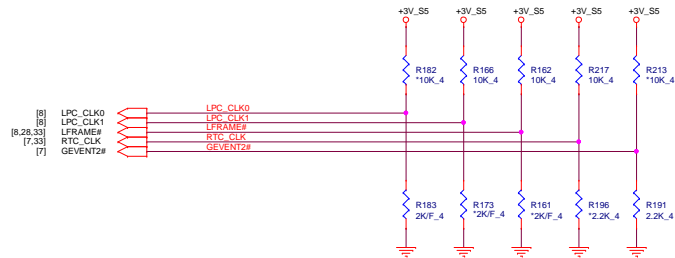
HUB3

W25Q32BVSSIG:AKE391P0N00  
W25Q64FVSSIG:AKE3EFP0N07

RevB 1225 Change from 8M to 4M

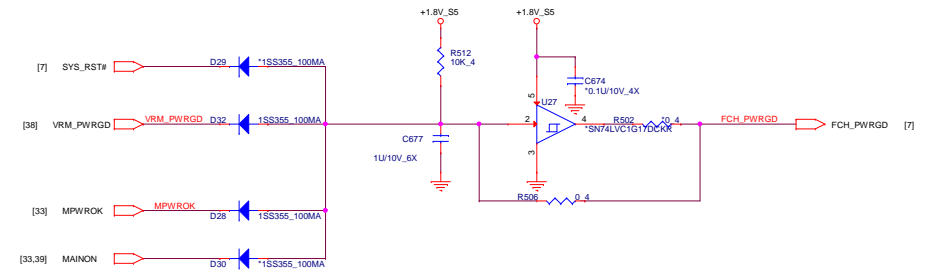


## STRAPS PINS



## REQUIRED STRAPS

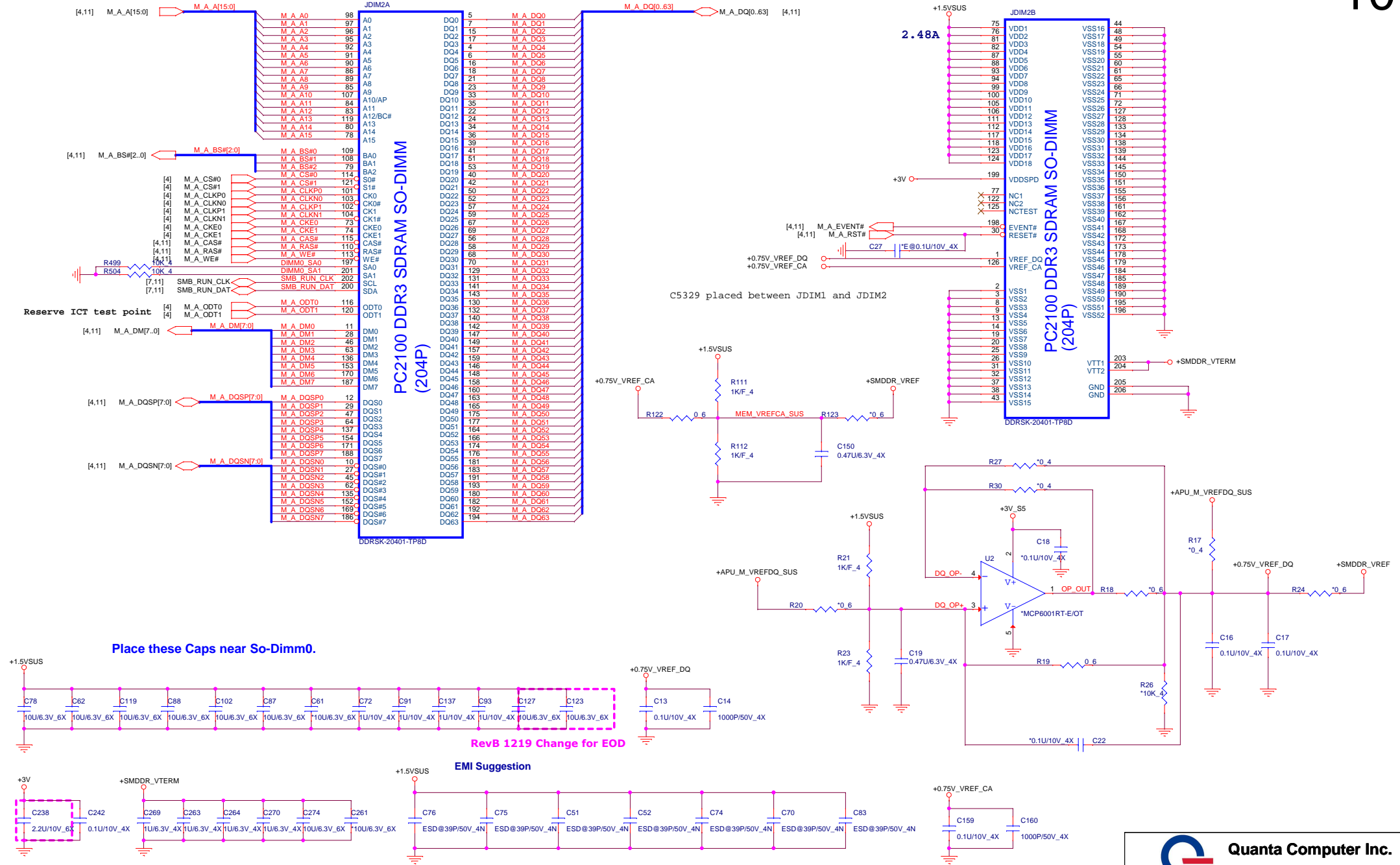
	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2#
<b>PULL HIGH</b>	BOOT Fail Timer ENABLE	Internal CLKGEN ENABLE <b>DEFAULT</b>	SPI ROM <b>DEFAULT</b>	Normal Power Timing ENABLE <b>DEFAULT</b>	SPI Voltage 1.8V <b>DEFAULT</b>
<b>PULL LOW</b>	BOOT Fail Timer DISABLE <b>DEFAULT</b>	Internal CLKGEN DISABLE	LPC ROM	Normal Power Timing DISABLE	SPI Voltage 3.3V <b>DEFAULT</b>



## PWRGD CIRCUIT

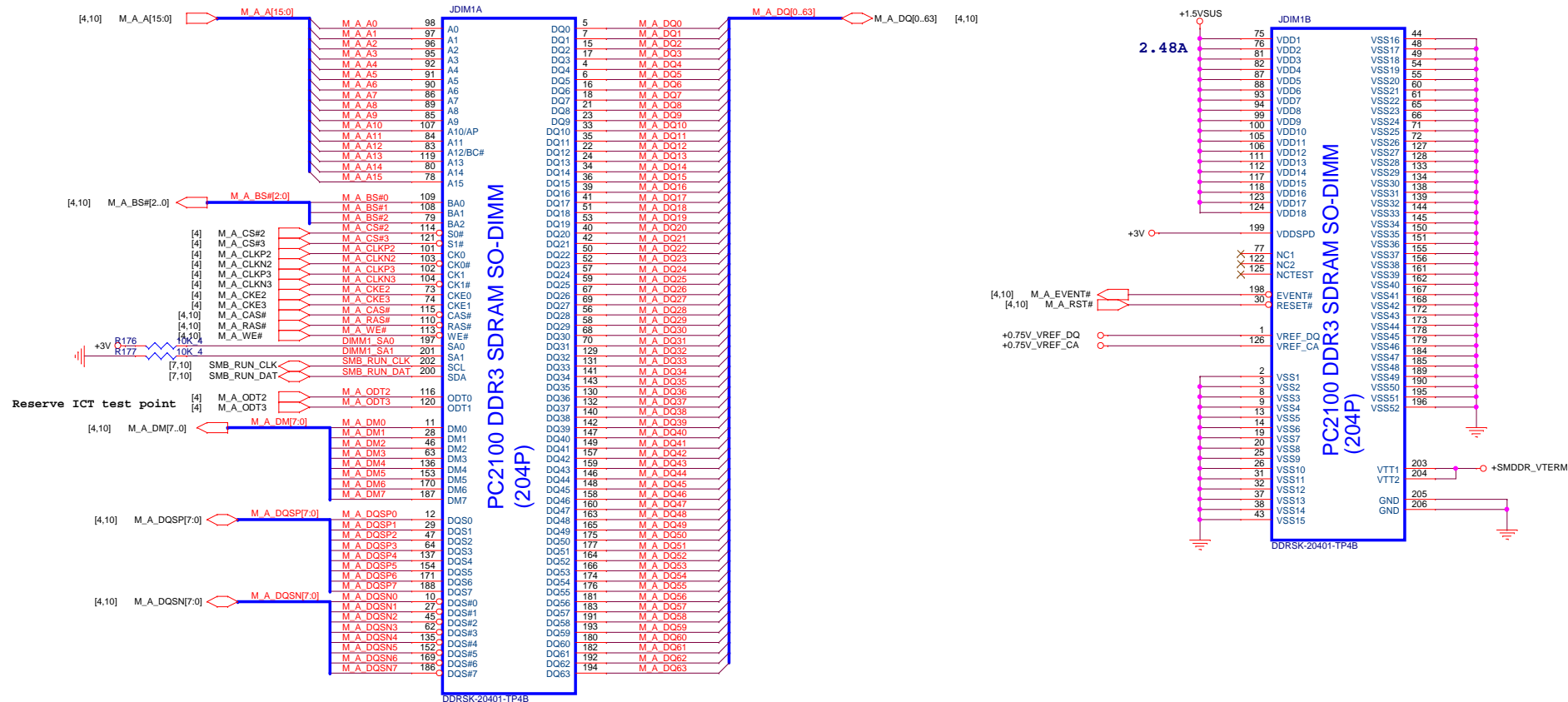
# DDR\_STD(DDR)

10

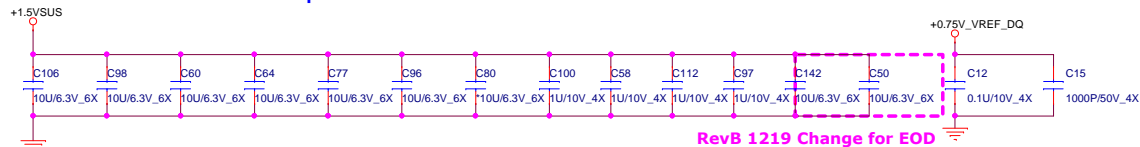


# DDR\_STD(DDR)

11

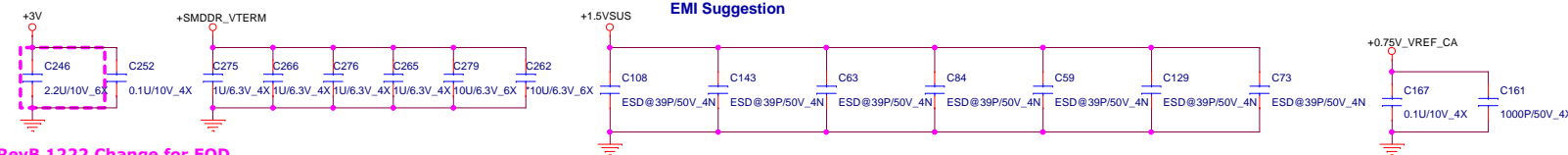


Place these Caps near So-Dimm0.



RevB 1219 Change for EOD

EMI Suggestion



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PROJECT : BD9

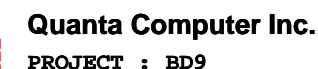
Size	Document Number	Rev
	DDR3 DIMM-1	A1A
Date:	Tuesday, December 25, 2012	Sheet 11 of 41



1 => +3V\_GPU  
2 => +VDDC,+VDDCI,+1.5V\_GPU,+0.95V\_GPU  
3 => +1.8V\_GPU

Intel platform: Lane0 ~ Lane15  
Brazos platform: Lane12 ~ Lane15  
Comal and Sabine platform: Lane8 ~Lane15  
Richland and Kabini platform: Lane0 ~ Lane7

Timing diagram for the reset sequence of the PFG Space Ready signal. The diagram shows the relationship between several signals: +5VRUN/+3VRUN/VDDR3, RUNPWROK, MVDDQ/VDDC/VDDCI 1.8V\_IO/PCIE\_VDDC, PWRGOOD, PCIE\_RST#(PERSTB), and PCIE Clock. The sequence starts with a reset pulse on PCIE\_RST#(PERSTB) and PCIE Clock. After the reset, PWRGOOD becomes active, followed by RUNPWROK. The PCIE Clock then transitions from a dashed state to a solid state. The diagram includes timing constraints: 20ms max for the initial reset pulse, 100ms min for the PWRGOOD pulse, and 100us min for the PCIE Clock pulse. The diagram is labeled "ASIC in Reset", "Hardware Reset Sequence", and "PFG Space Ready".

 PROJECT : BD9

**Mars M2/ PEG\*8**

Size	Document Number	Rev
	<b>Mars_M2/ PEG*8</b>	A1
Date:	Tuesday, December 25, 2012	Sheet 12 of 41

### System Memory Aperture size

	PS0[3:1] ROMIDCFG[2:0]
128M	000
256M	001
64M	010
Reserved	011

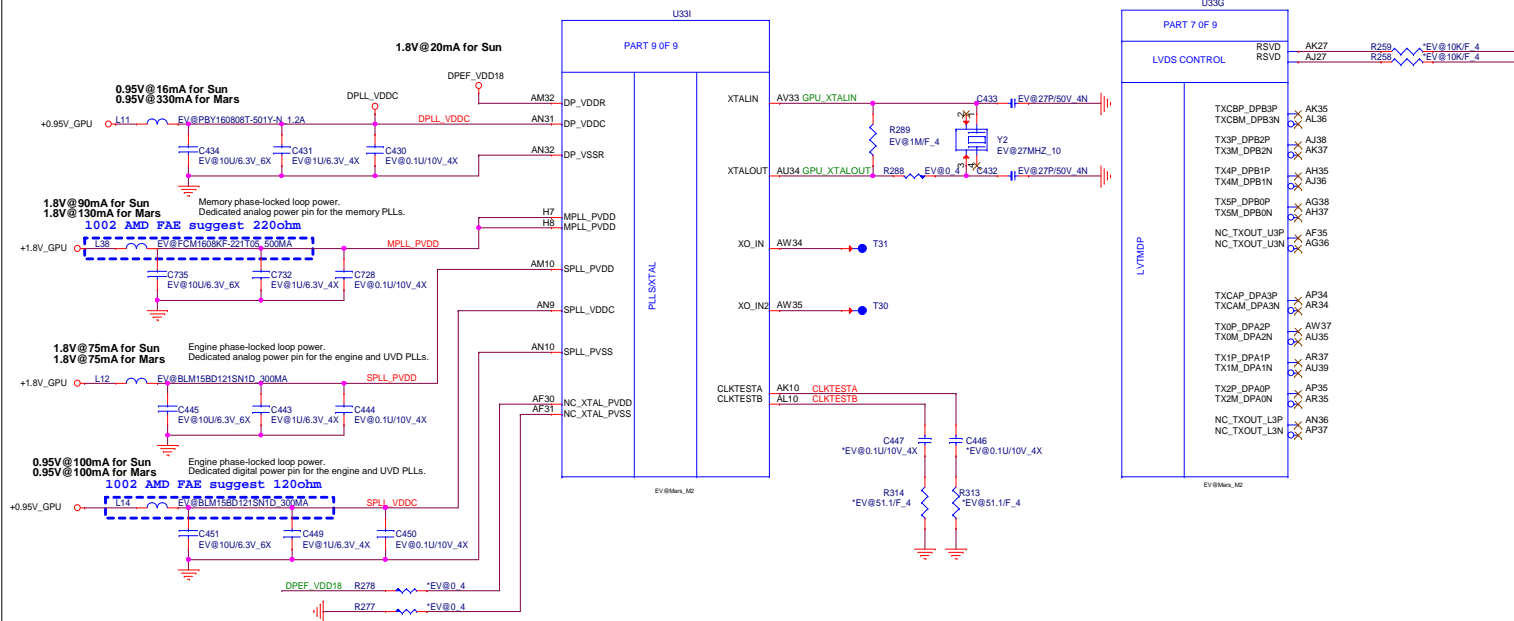
## MLPS

R <sub>pu</sub>	R <sub>pd</sub>	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

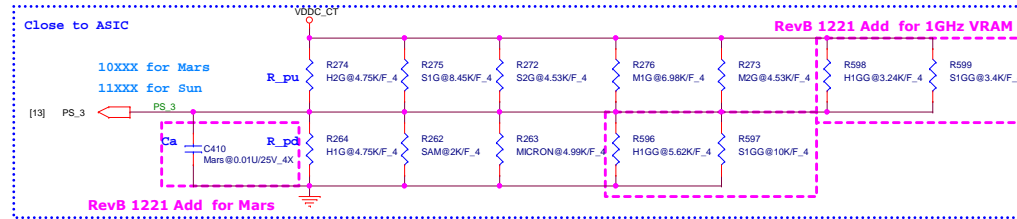
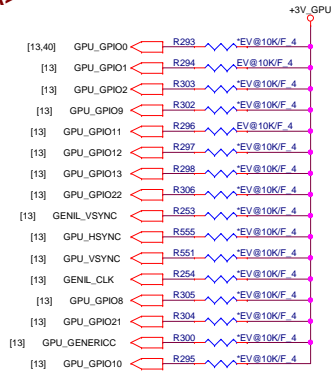
Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00 X CH4681JEB00 X
82nF	01	CH3823K1B00
10nF	10	CH31003KB1
NC	11	

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	01000
PS_3	11XXX



## &lt;VGA&gt;



## MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

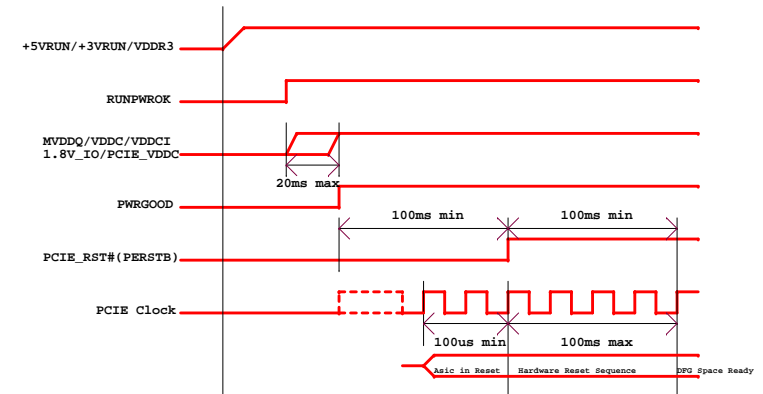
## DDR3 Memory TYPE

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

Vendor	Vendor P/N	B/S P/N (QC1 P/N)	Size	MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW16 * 4	1GB	000
	H5TC4G63AFR-11C (256M*16)	AKD5PGWTW05 * 4	2GB	111
Micron	MT41J128M16JT-107G:K (128M*16)	AKD5DGSTL00 * 4	1GB	011
	MT41K256M16HA-107G:E (256M*16)	AKD5PGSTL00 * 4	2GB	100
Samsung	K4W2G1646E-BC11 (128M*16)		1GB	001
	K4W4G1646B-HC11 (256M*16)		2GB	010

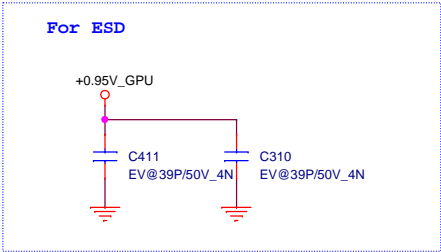
CONFIGURATION STRAPS -- SEE EACH DATABASE FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
STRAP_TX_CFG_DRV_FULL_SWING	PS_1[4]		Control the transmitter full-half- swing mode 0: 50% Tx output swing 1: Full Tx output swing	1
STRAP_TX_DEEMPH_EN	PS_1[5]		PCIe transmitter, de-emphasis enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
STRAP_BIF_GEN3_EN_A	PS_1[1]		PCIe GEN3 Capability 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	0 for Kabini
STRAP_BIF_VGA_DIS	PS_2[4]		VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space) 0: VGA controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
ROM_CONFIG[2:0]	PS_0[3..1]		Serial ROM type or Memory Aperture Size Select  If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
STRAP_BIOS_ROM_EN	PS_2[3]		Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
N/A	PS_0[4]		Reserved for internal use only. Must be 1 at reset	1
N/A	PS_1[3]	GENLK_CLK	Reserved	0
STRAP_BIF_CLK_PM_EN	PS_1[2]	GPIO8	PCIe reference clock power management capability is reported in the PCI 0: The CLKREQ power management capability is disabled 1: The CLKREQ power management capability is enabled	0
RESERVED RESERVED	NA NA	GPIO21 GENERICC	Reserved Reserved (for Thames/Whistler/Seymour only)	0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

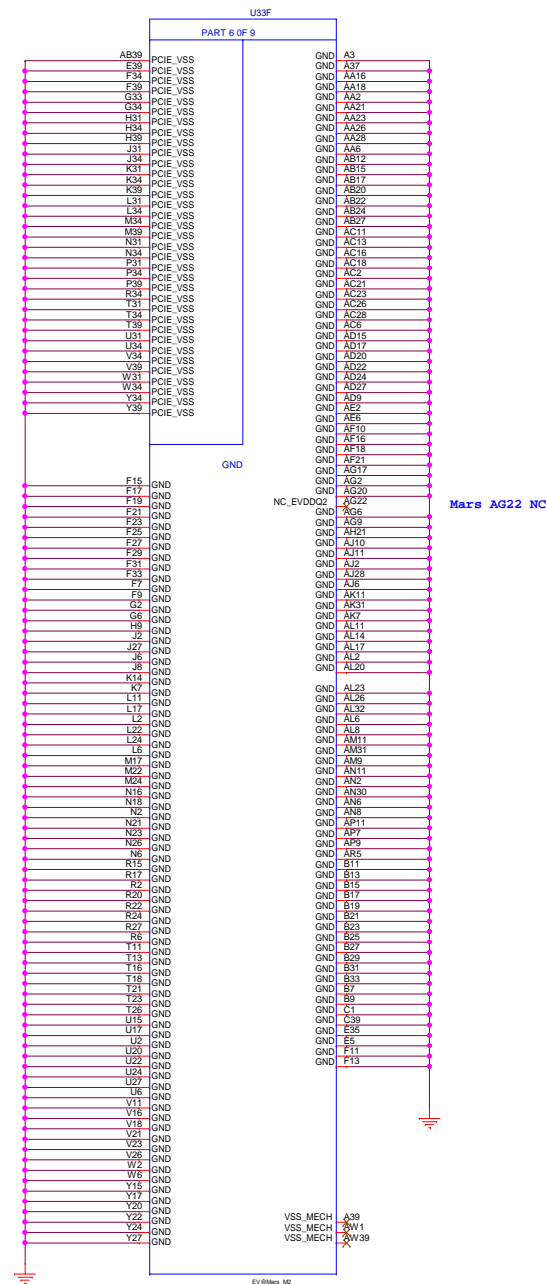
## Power Up Reset Sequence

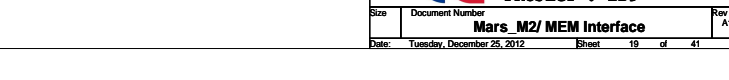
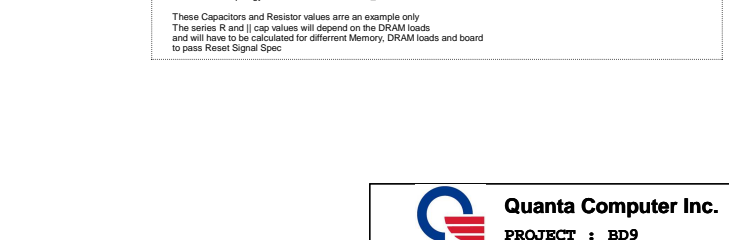
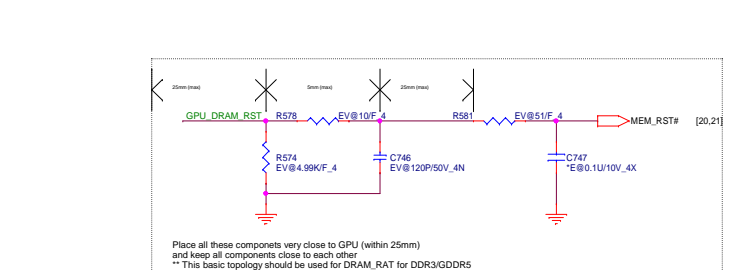
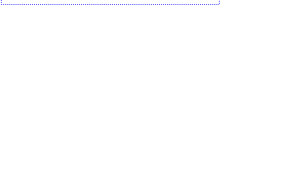
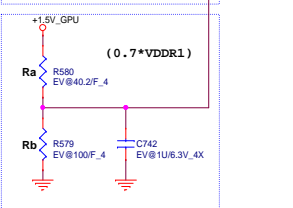
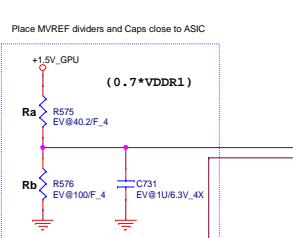
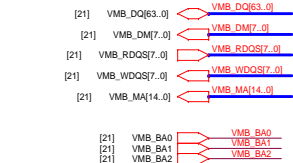
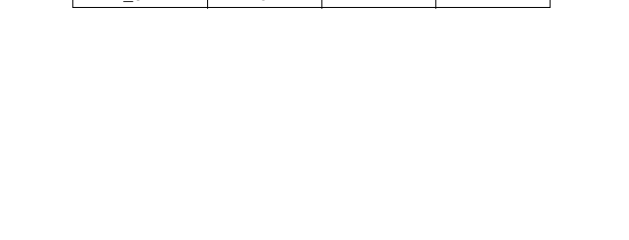
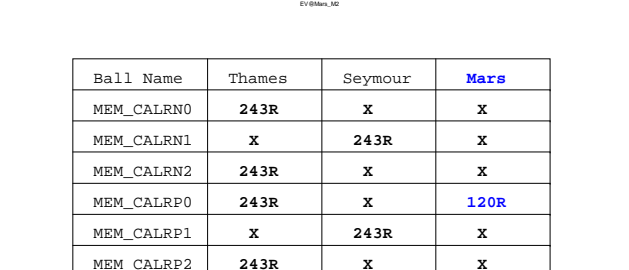
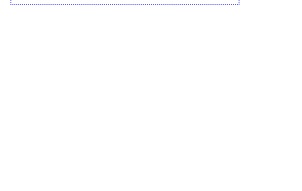
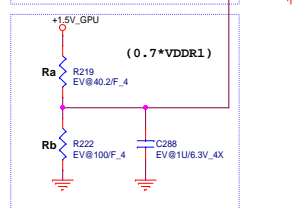
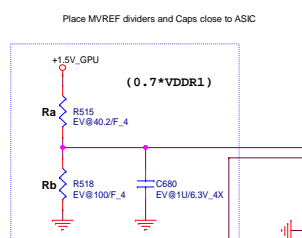
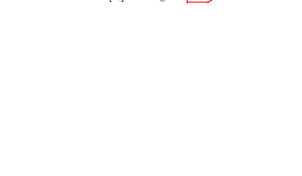
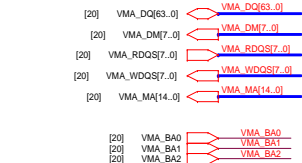




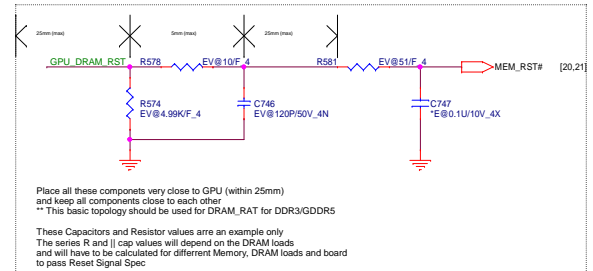








Ball Name	Thames	Seymour	Mars
MEM_CALRN0	243R	X	X
MEM_CALRN1	X	243R	X
MEM_CALRN2	243R	X	X
MEM_CALRP0	243R	X	120R
MEM_CALRP1	X	243R	X
MEM_CALRP2	243R	X	X



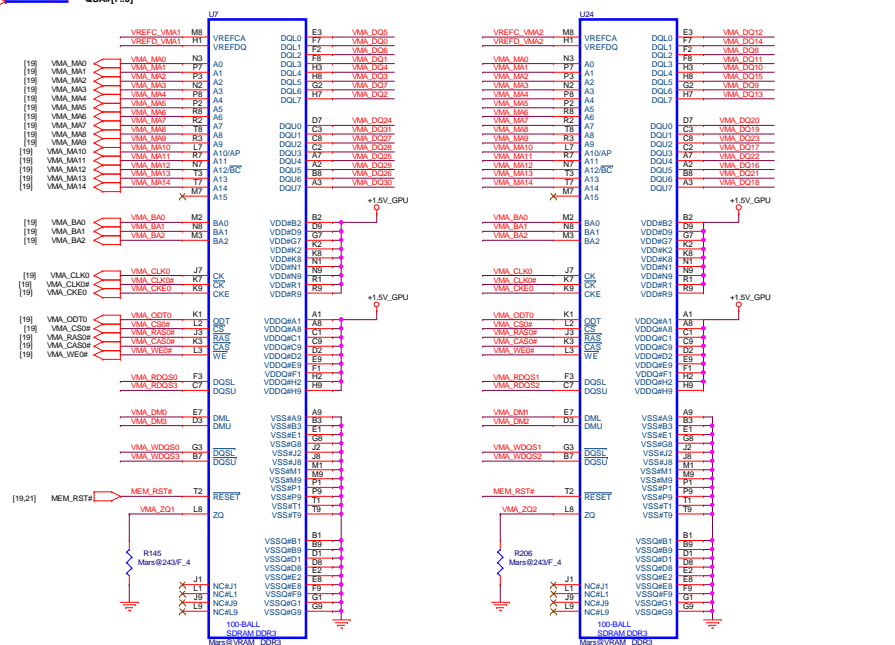
Place all these components very close to GPU (within 25mm) and keep all components close to each other  
 \*\* This basic topology should be used for DRAM\_RAT for DDR3/GDDR5  
 These Capacitors and Resistor values are an example only  
 The series R and C cap values will depend on the DRAM loads and will have to be calculated for different Memory, DRAM loads and board to pass Reset Signal Spec

## CHANNEL A: 1024MB DDR3 (128M\*16\*4pcs) &lt;VGA&gt;

[19] VMA\_DQ[63..0] VMA\_DQ[63..0]  
 [19] VMA\_DM[7..0] VMA\_DM[7..0]  
 [19] VMA\_RDS[7..0] VMA\_RDS[7..0]  
 [19] VMA\_WDS[7..0] VMA\_WDS[7..0]

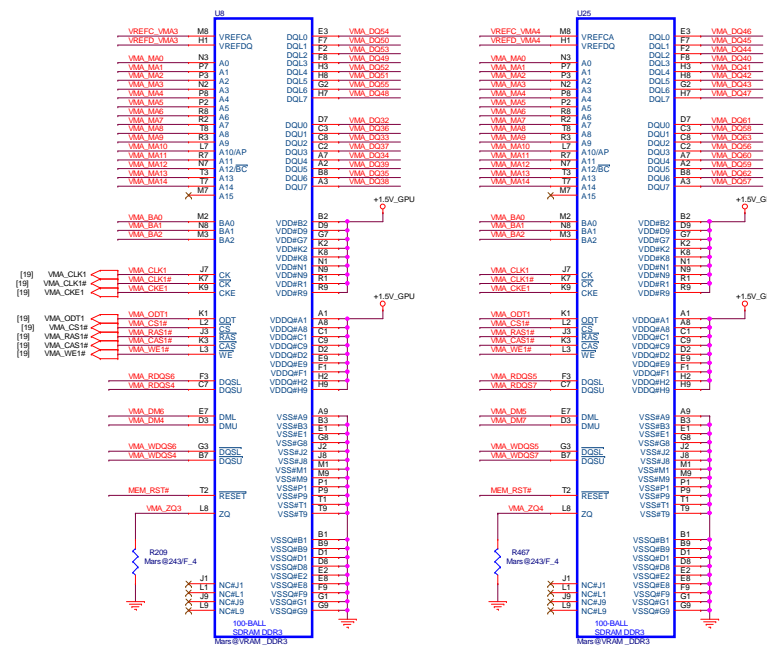
QSA[7..0]

QSA[7..0]



TOP Left

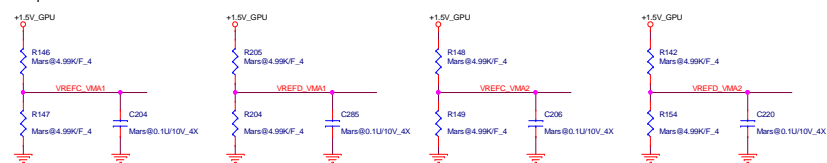
BOT Left



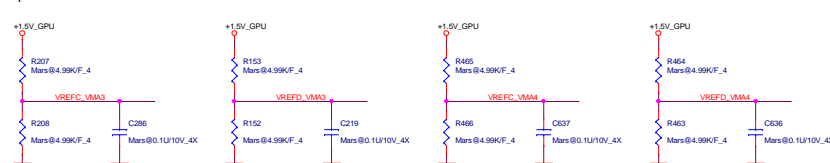
BOT Right

TOP Right

## Group-A0 VREF

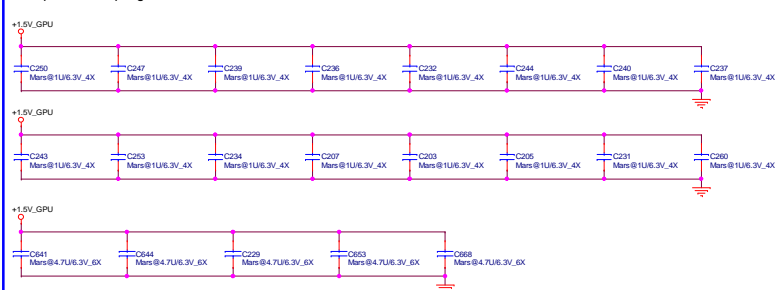


## Group-A1 VREF

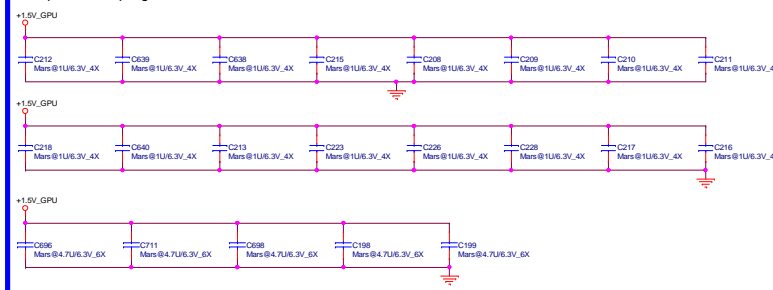


## MEM\_A0 CLK

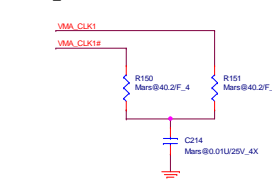
## Group-A0 decoupling CAP



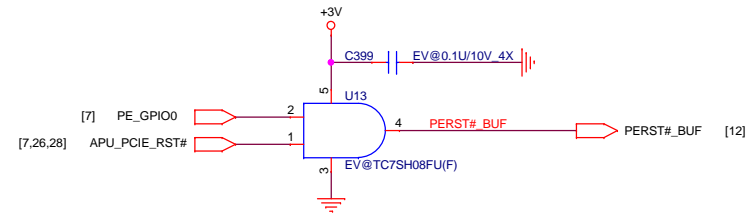
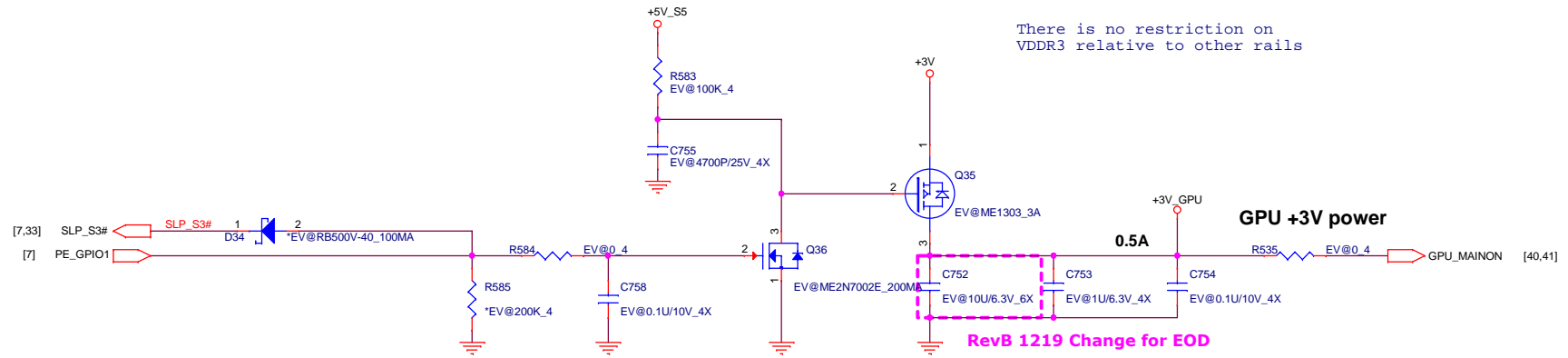
## Group-A1 decoupling CAP



## MEM\_A1 CLK







Quanta Computer Inc.

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Mars\_M2/ PX5

Rev

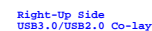
A1A

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<USB> <U3B>



	Charger , AM
	Charger , FM
	USB , PM
	USB , CM


	Charger , AM2
	Charger , FM
	USB , PM
	USB , CM

	Charger , AM
	Charger , AP
	USB , PM
	USB , CM

	Charger , AM
	USB , PM
	USB , CM

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 <b>Quanta Computer Inc.</b> <b>PROJECT : BD9</b>		
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Close to Pin1

APU\_PCIE\_RST#

or vendor suggestion

25m11

GIGA:AR8161B  
10/100:AR8162B

0920 FAE suggest remove 49.9K, 0.1u and 1000p

**For ESD**

The diagram shows the pin configuration for the LAN8710S04AD0 chip, which is a 16-pin package. The pins are numbered 1 through 16. The ESD protection pins are highlighted in red. The pins are:

- Pin 1: TX0P
- Pin 2: GND
- Pin 3: TX0N
- Pin 4: CH3
- Pin 5: VDD
- Pin 6: TX1P
- Pin 7: TX1N
- Pin 8: LAN\_VDD33
- Pin 9: CH4
- Pin 10: CH2
- Pin 11: CH1
- Pin 12: TX2P
- Pin 13: TX2N
- Pin 14: TX3P
- Pin 15: TX3N
- Pin 16: TX4P

The chip is labeled "LAN8710S04AD0" and "U1".

RevA 1114 Add Gas Tube for Surge issue  
RevC 0130 Un-stuff D4,D5

Diagram illustrating the structure of the CN14 gene and its expression patterns across various tissues. The gene structure shows 8 exons (red boxes) and 7 introns (green lines). The tissues and their corresponding expression levels are:

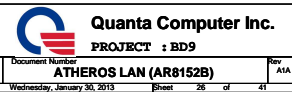
Tissue	Expression Level
NC4/3	8
NC3+/	7
Rx/1+	6
NC2/2	5
NC1/2+	4
Rx/1+	3
Tx/0	2
Tx/0+	1

The gene is located on chromosome 10 (10p11.23). The expression levels are indicated by the number of red boxes in the tissue column.

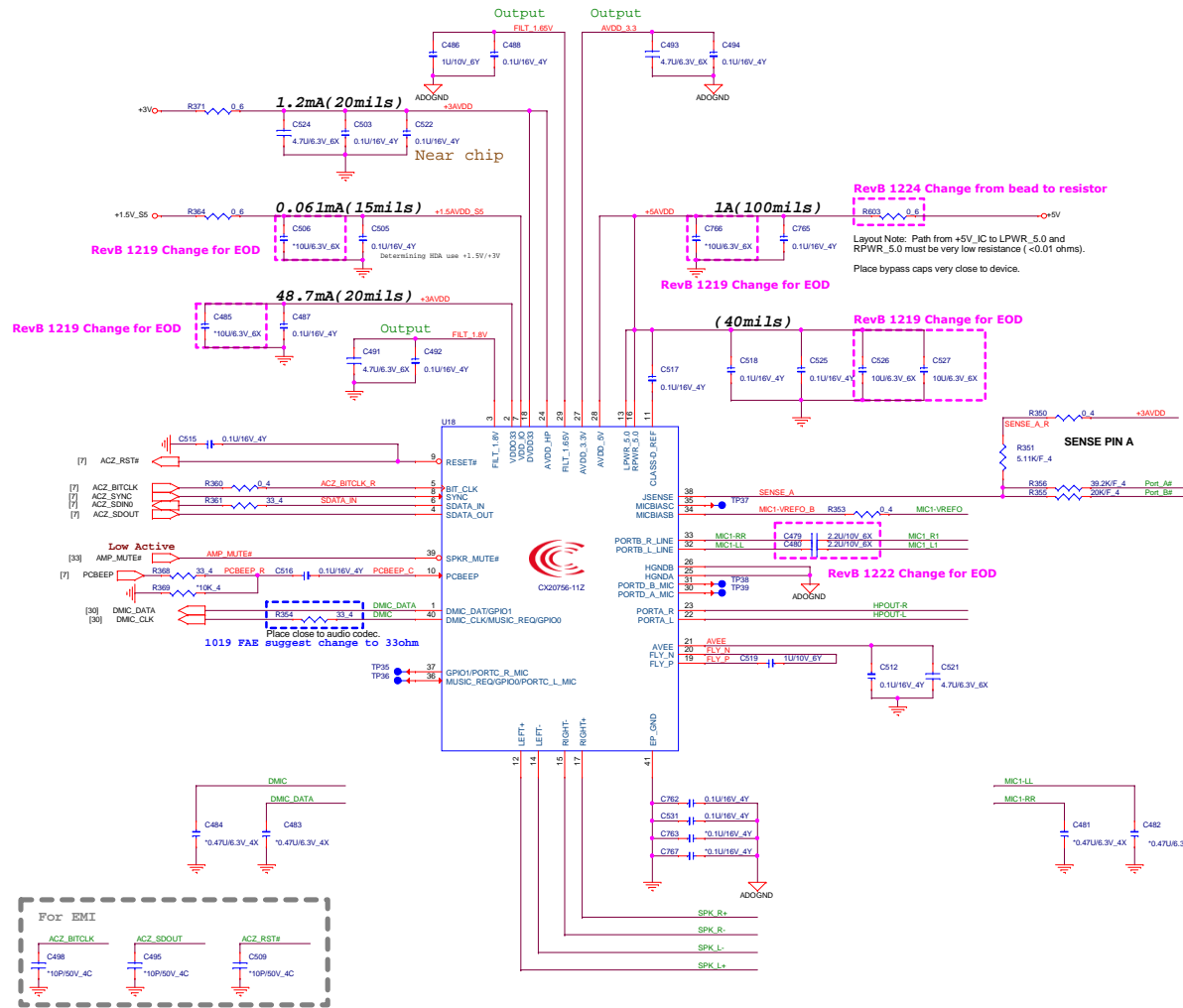
LED0 = LAN_ACTLED	1	High core voltage(default=1)
	0	Low core voltage
LED1 = LAN_LINKLED#	1	Switch mode regulator (SWR) select
	0	Linear regulator (LDO) select
LED2	1	25 MHz external clock input
	0	48 MHz external clock input

Power on Strapping pin

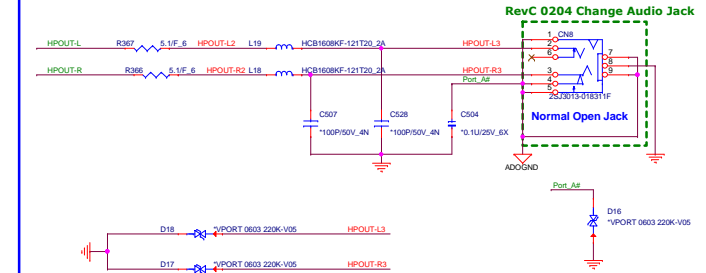
The diagram shows two signal lines, LAN\_ACTLED and LAN\_LINKLED#, each connected to a 5.1K resistor (R521 and R516 respectively) which is then connected to a 5.1K pull-up resistor to ground.



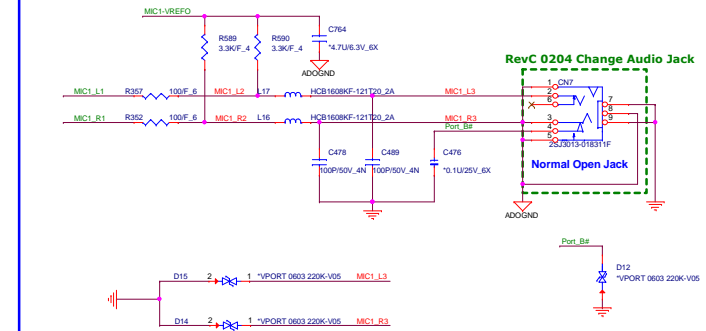
**Codec (CX20756-11Z)** <ADO> <EMI>



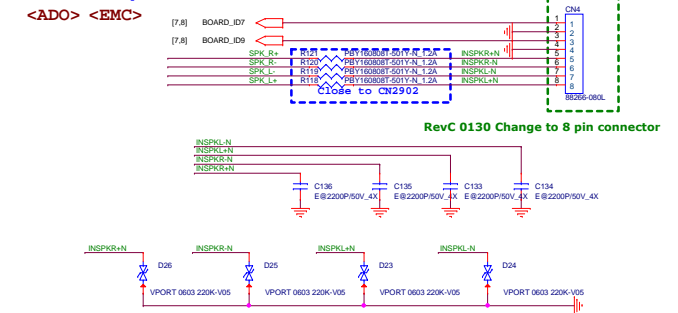
HP <ADO> <EMC>



**External MIC** <ADO> <EMC>

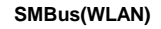


### Internal Speaker

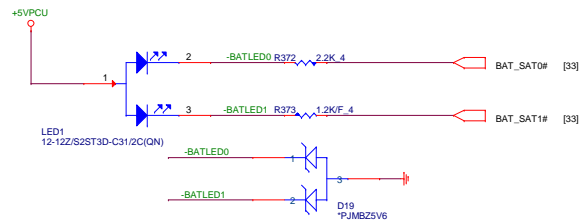


RevB 1219 Change

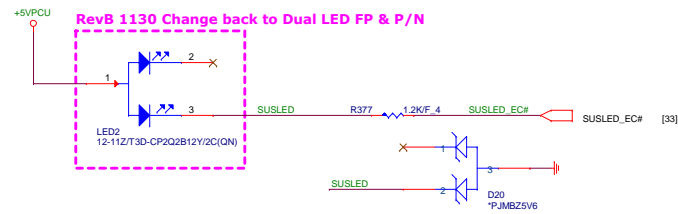
**RevB 1219 Change for EOD**



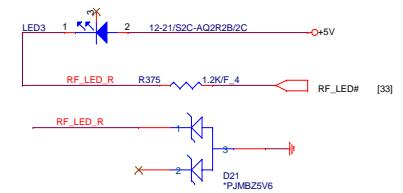
## BATTERY



## POWER

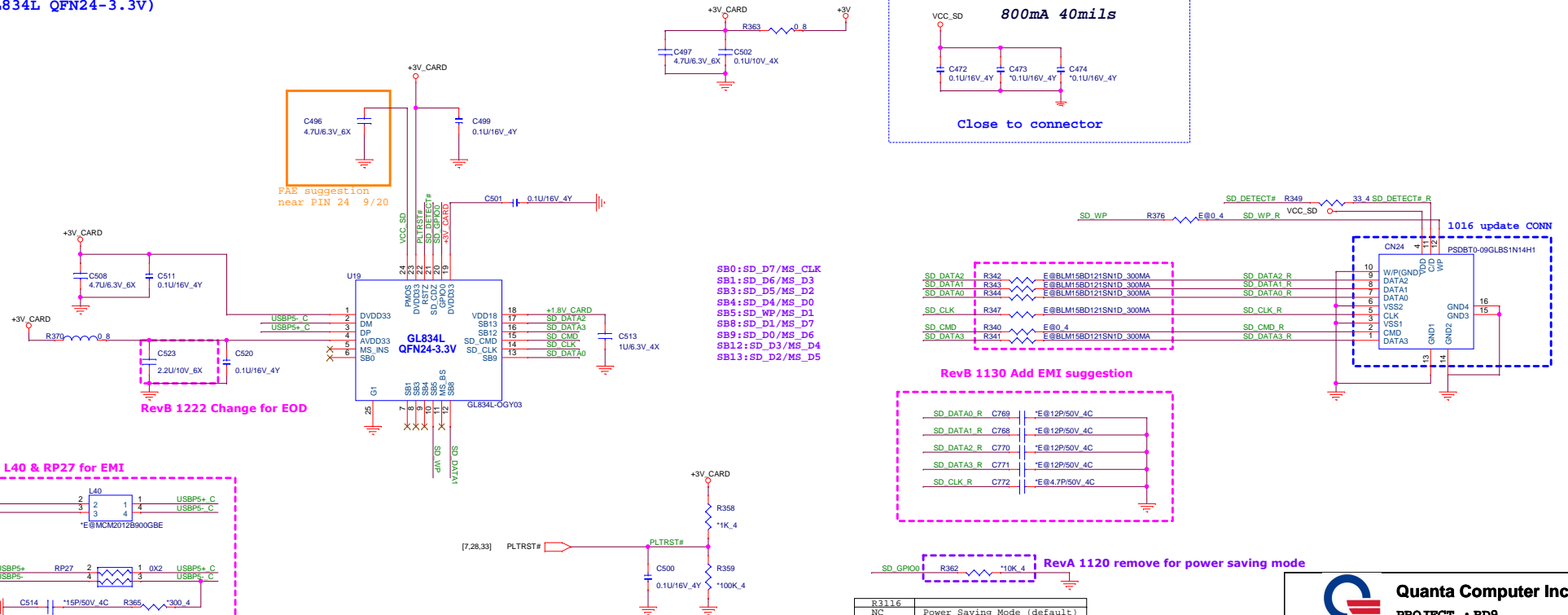


## RF LED



**2 IN 1 CARD READER (Type: MS/SD) <MMC>**

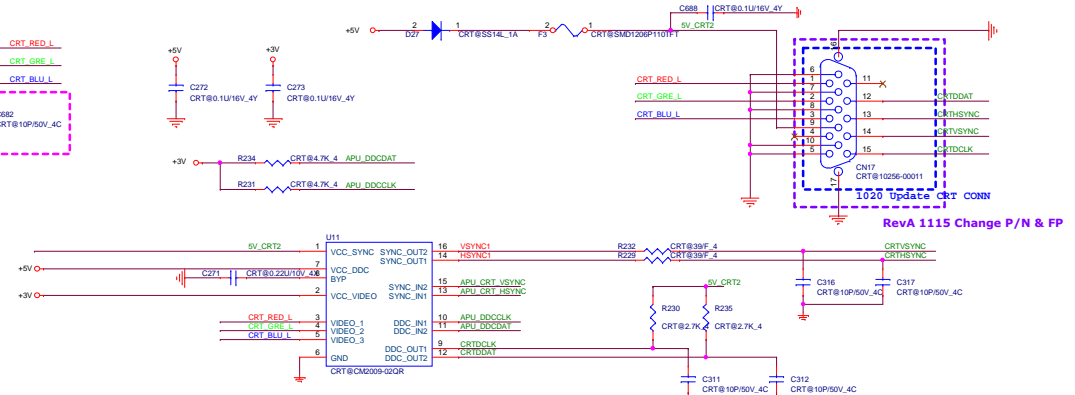
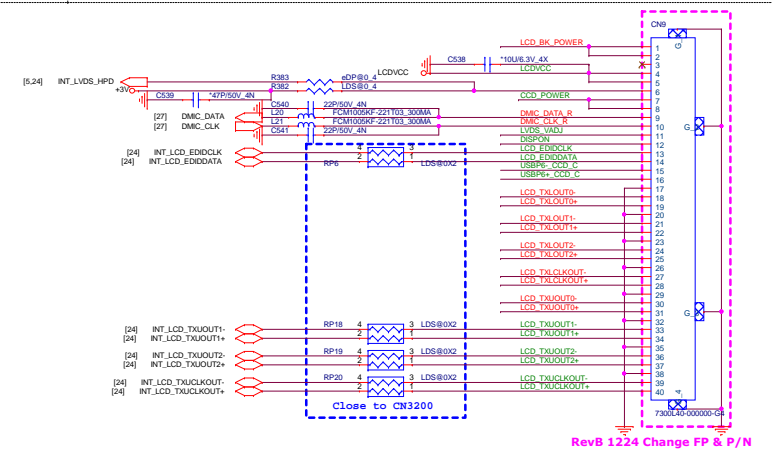
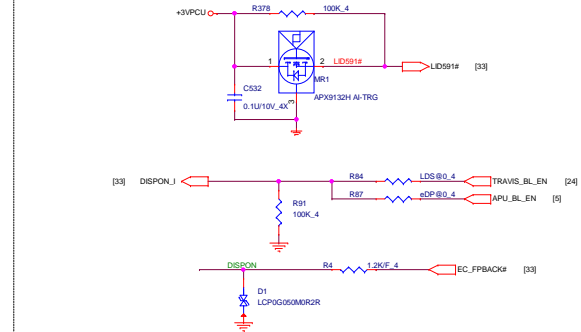
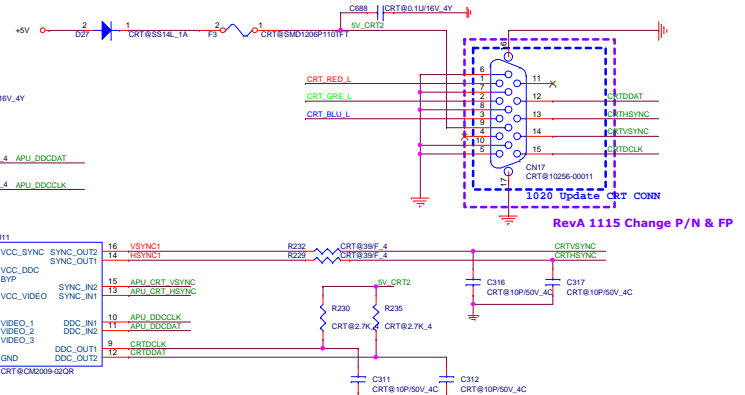
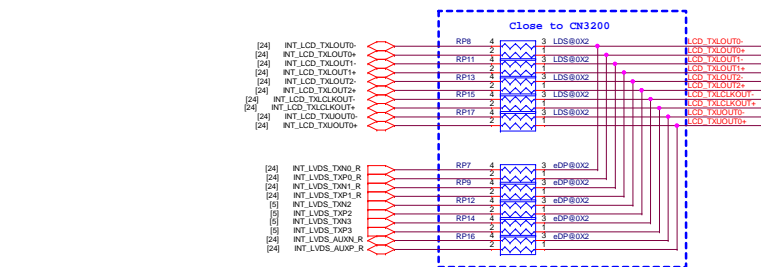
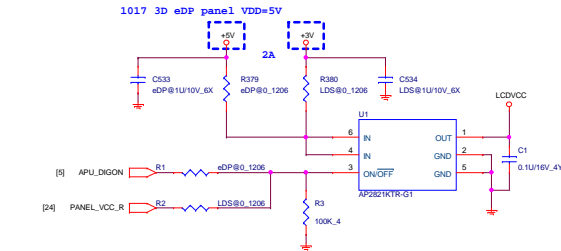
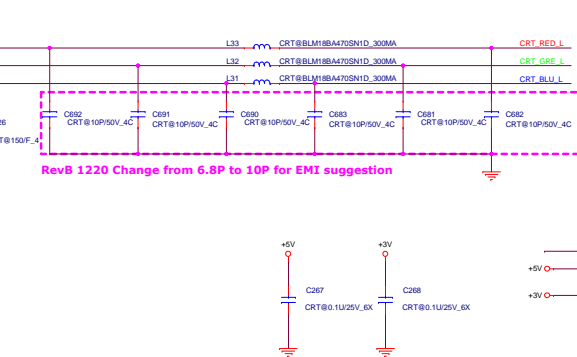
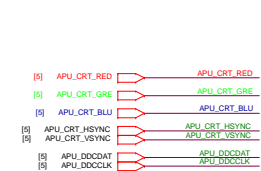
Card Reader (GL834L QFN24-3.3V)



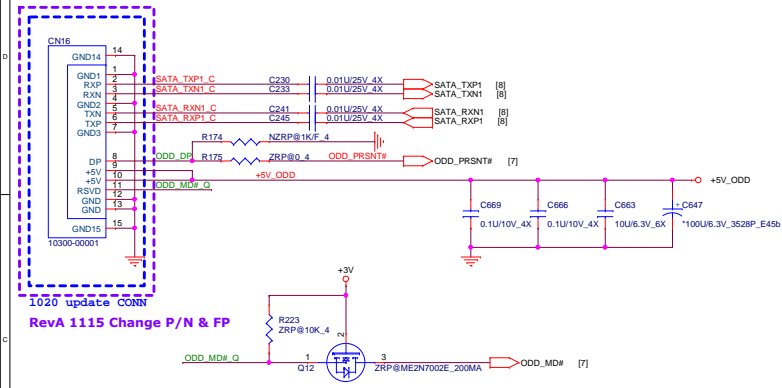
R3116	
NC	Power Saving Mode (default)
10K	Normal Mode



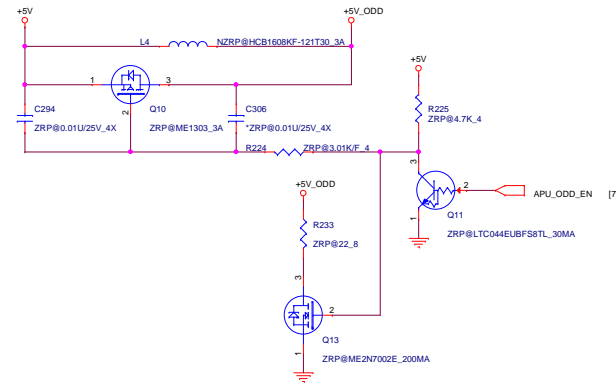
CRT [CRT]



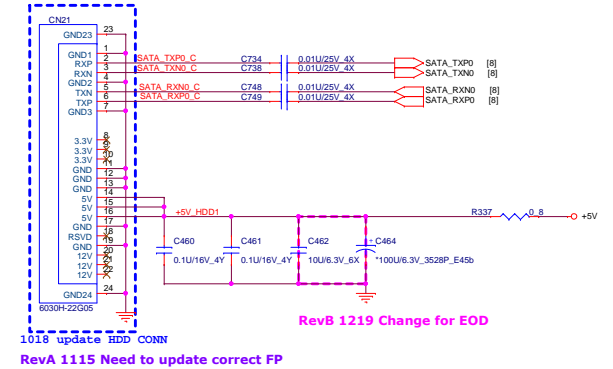
### SATA ODD [ODD]



### ODD Zero power <OZP>



### SATA HDD [HDD]



### 3D-LDO Power <GSR>

### 3D-u-micro P <GSR>

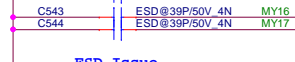
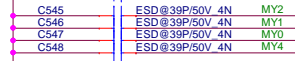
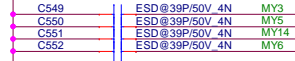
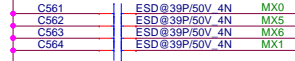
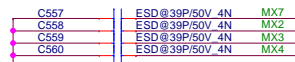
### 3D-SMBus <GSR>

### 3D-Sensor IC <GSR>

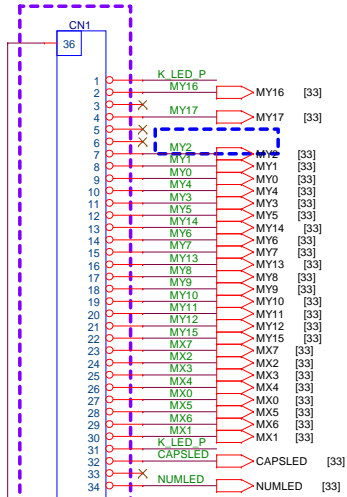
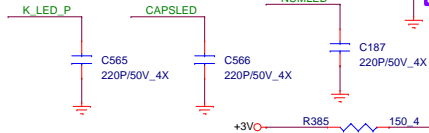
# KEY BOARD Connector <KBC> <EMI>

# TOUCH PAD BOARD <TPD> <EMI>

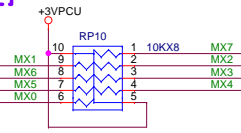
## INT KeyBoard



## ESD Issue



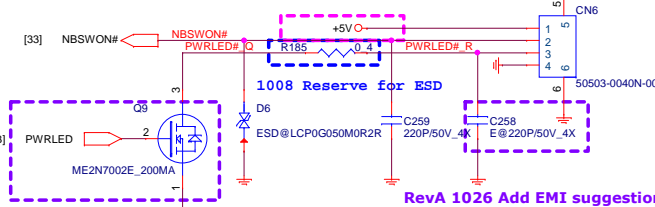
## RevA 1115 Change P/N



ID_Detect	default
Metal	+3.3V
TEXTURE	+5V

## Power Board (UIF) <PSW>

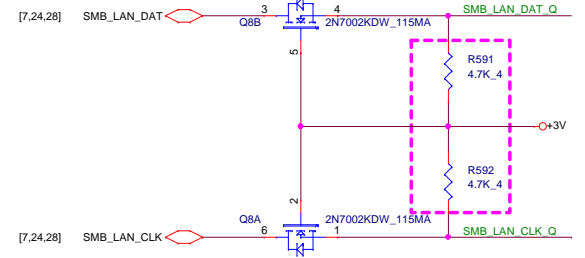
### RevB 1204 Change power rail from +5VPCU to +5V



### RevA 1114 Add Q3402 for PWRLED

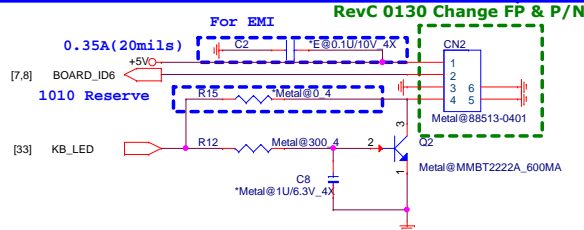
## TP board <TPD>

### RevB 1130 Add 4.7K PU

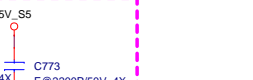
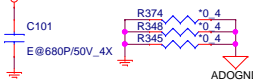
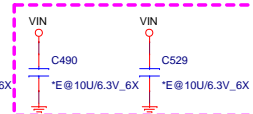


## KEY BOARD LED

### <KBP> <EMI>

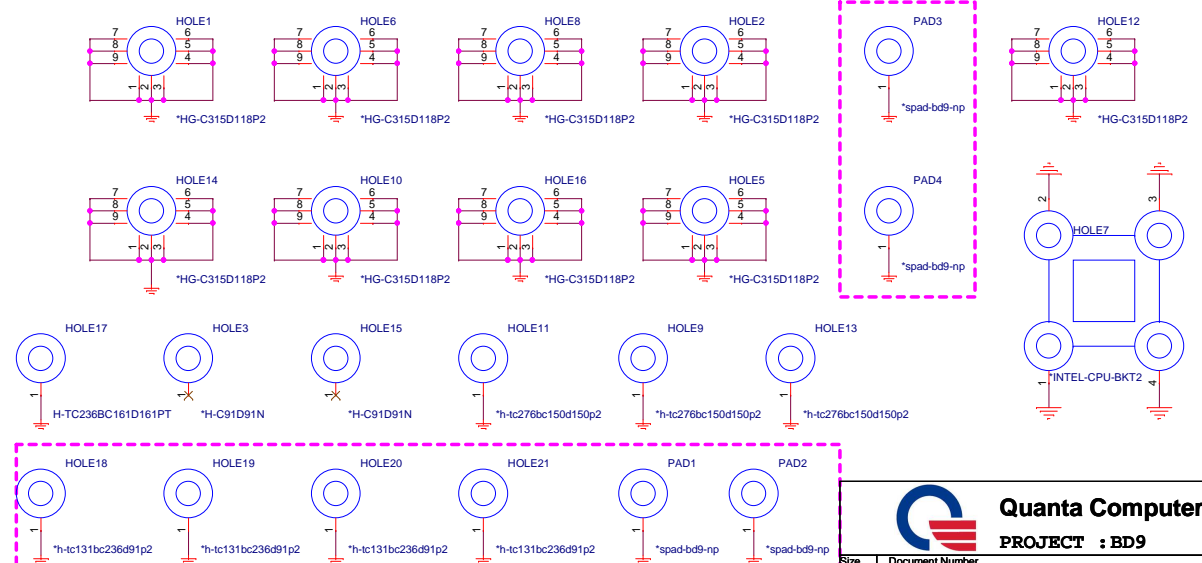


### RevB 1219 Change for EOD

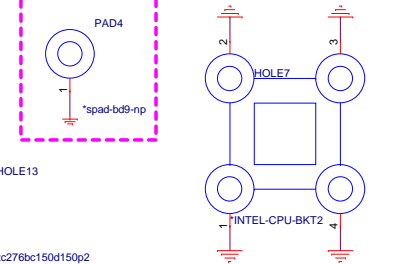
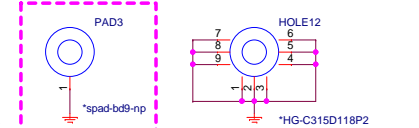


### RevB 1220 EMI solution

## HOLE <OTH>

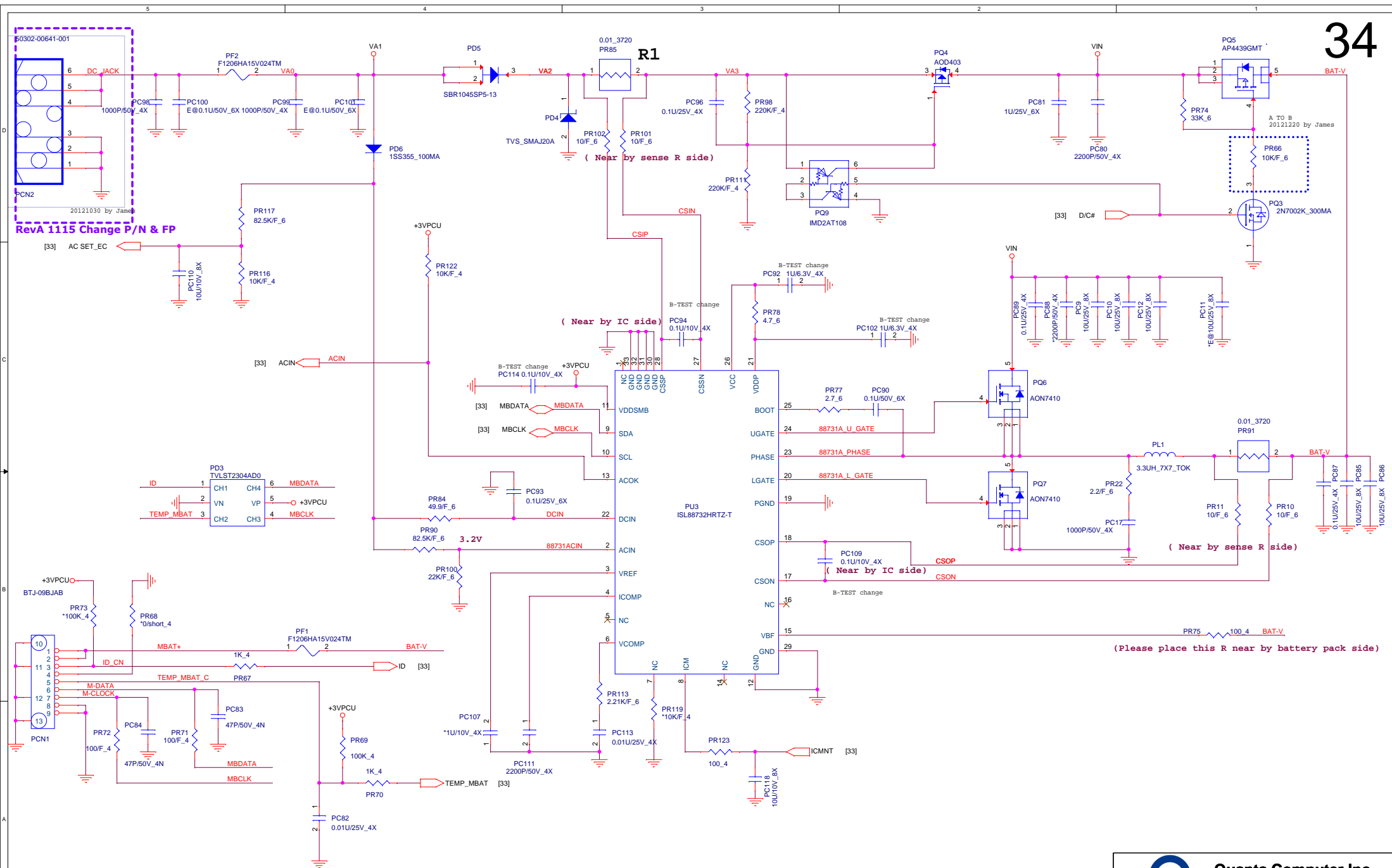


### RevB 1224 Remove Hole & Add PAD for ME





RevB 1204 Change power rail from +5VPCU to +5V

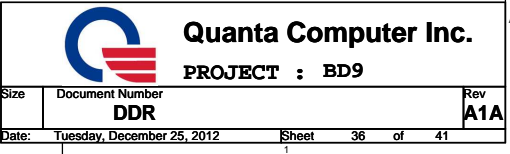


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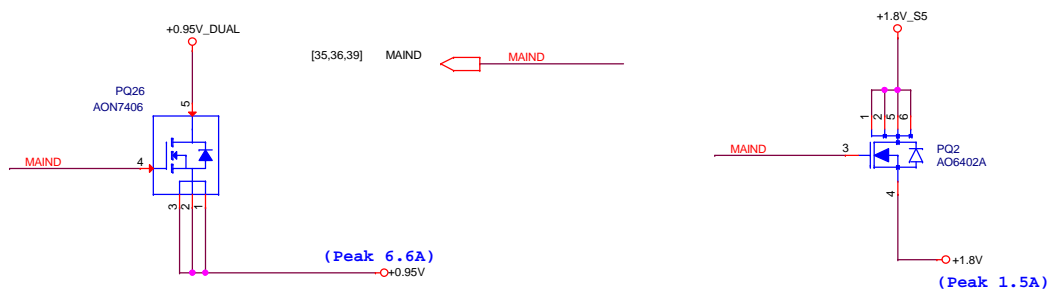
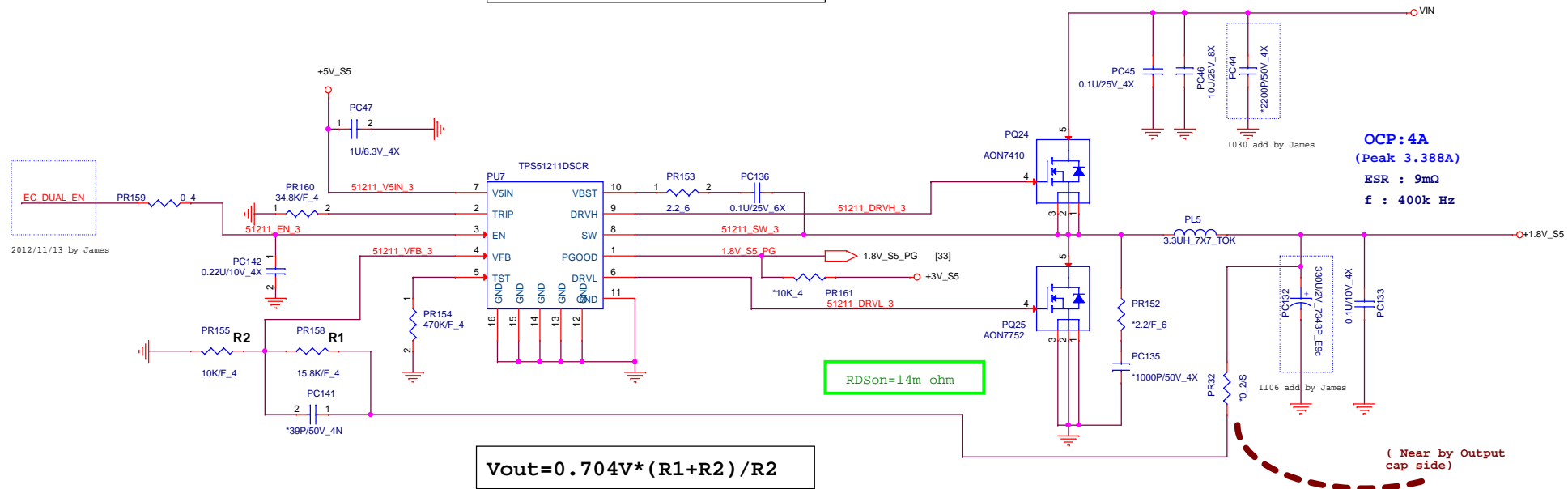
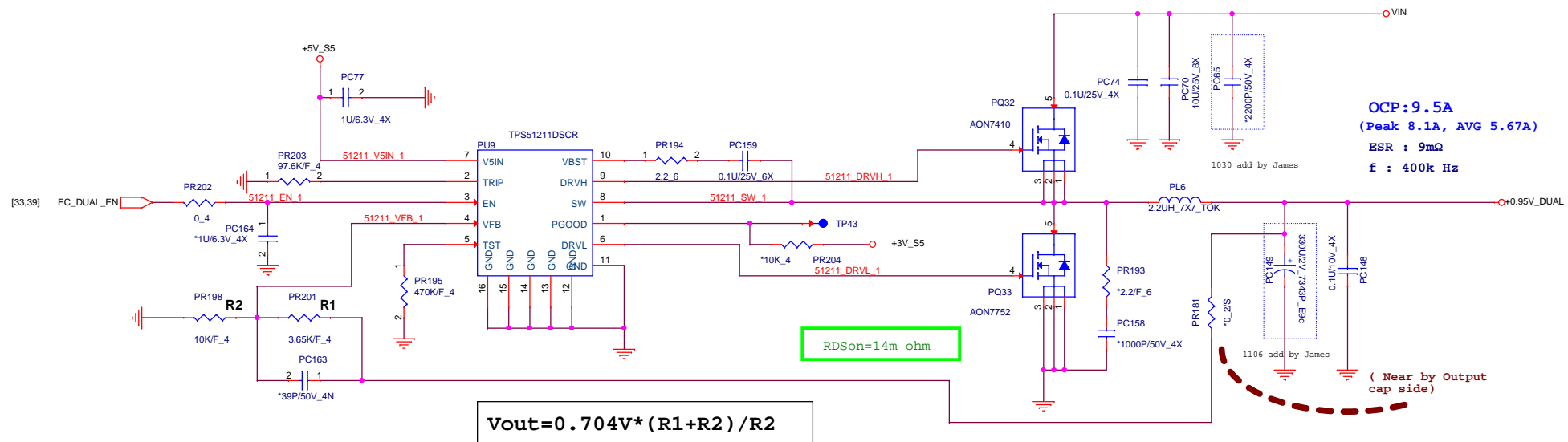
Size	Document Number	Rev
	<b>CHARGER-ISL88731C</b>	<b>A1A</b>

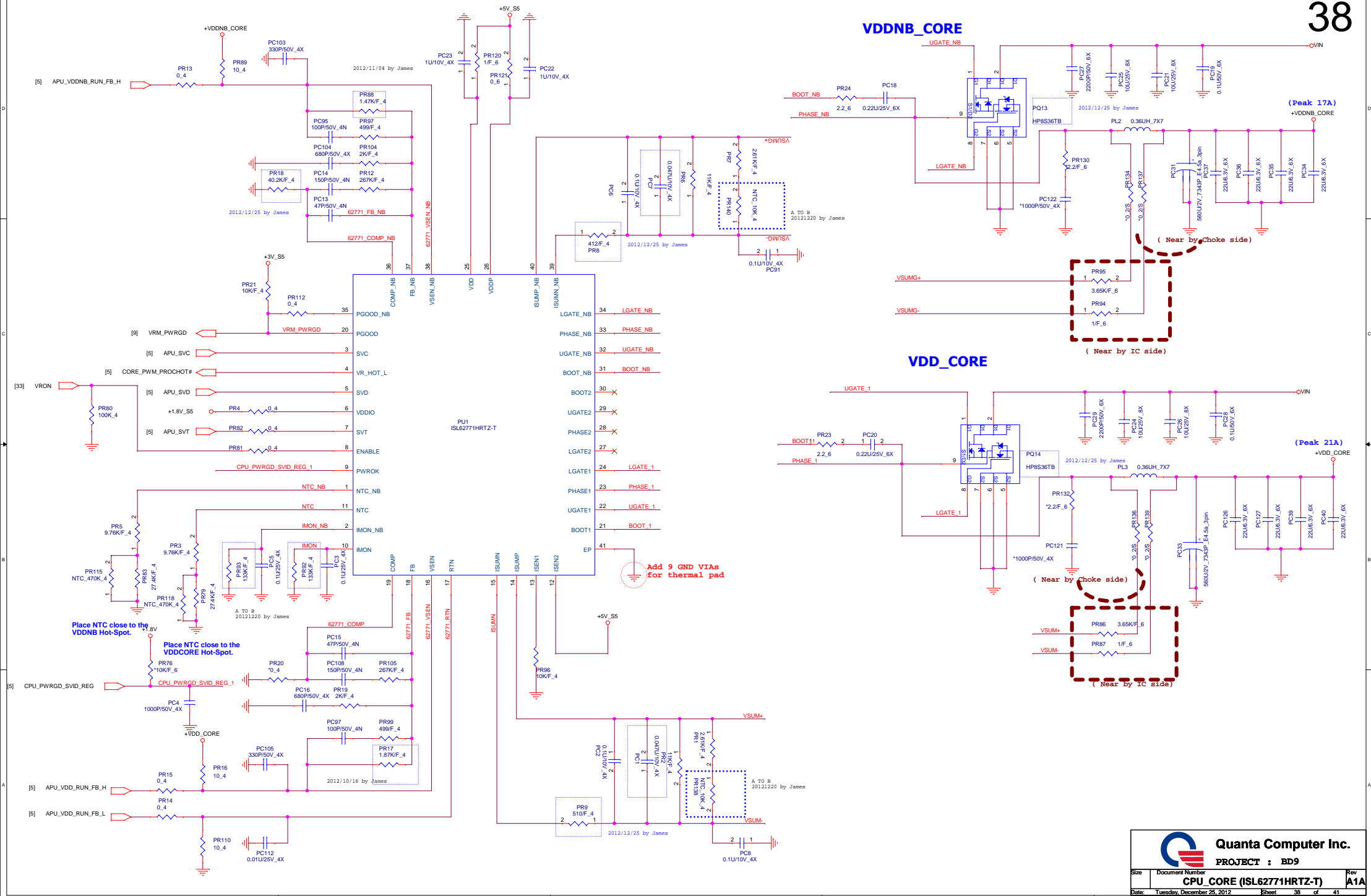
Date: Thursday, December 27, 2012 Sheet 34 of 41









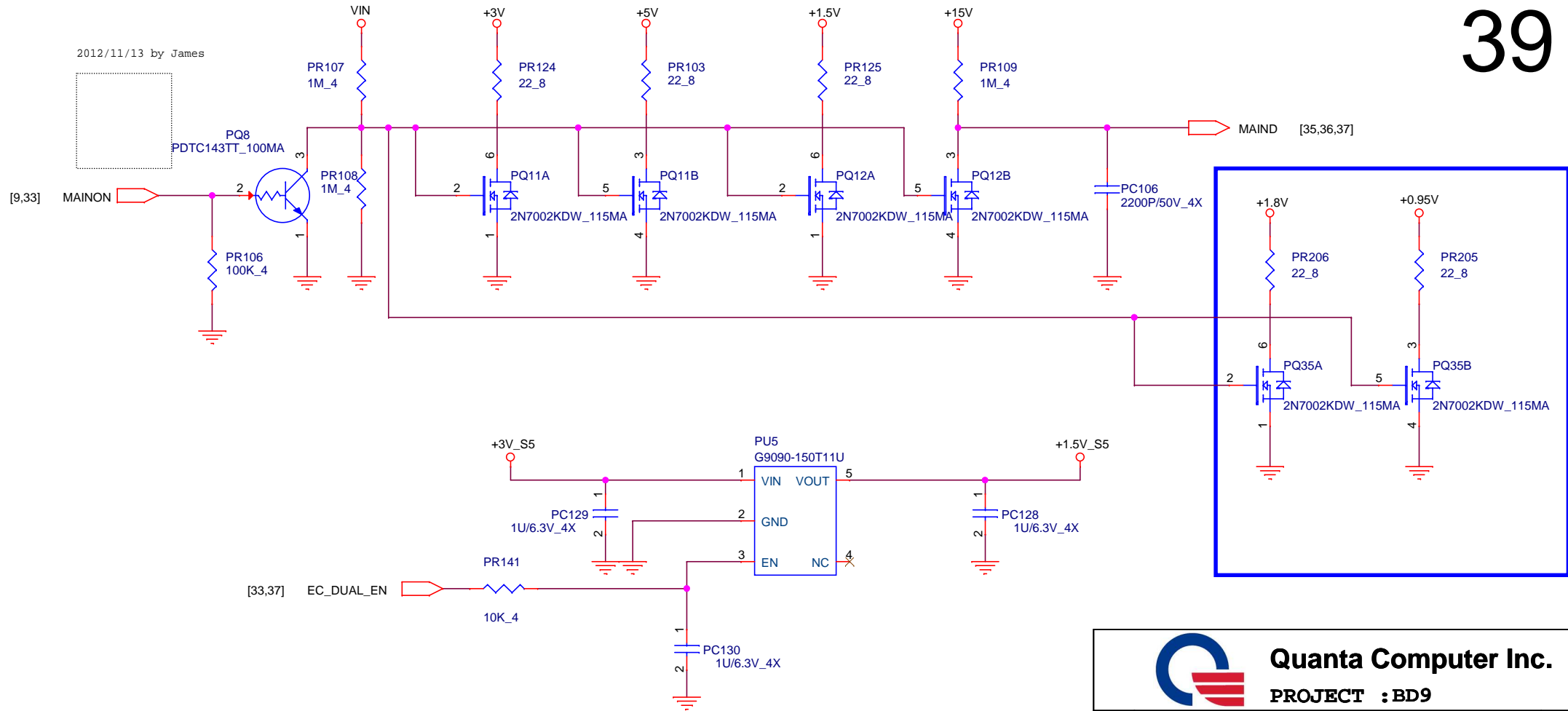


Quanta Computer Inc.

PROJECT : BD9

Size	Document Number	Rev
	<b>CPU CORE (ISL62771HRTZ-T)</b>	<b>A1A</b>
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2012/11/13 by James



**Quanta Computer Inc.**

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Size	Document Number	Rev
	<b>Discharge</b>	<b>A1A</b>

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VDDC(V)	GPFX_CORE_CNTRL5 (VID5)	GPFX_CORE_CNTRL4 (VID4)	GPFX_CORE_CNTRL3 (VID3)	GPFX_CORE_CNTRL2 (VID2)	GPFX_CORE_CNTRL1 (VID1)
1.175	0	1	1	0	1
1.150	0	1	1	1	0
1.125	0	1	1	1	1
1.100	1	0	0	0	0
1.075	1	0	0	0	1
1.050	1	0	0	1	0
1.025	1	0	0	1	1
1.000	1	0	1	0	0
0.975	1	0	1	0	1
0.950	1	0	1	1	0
0.925	1	0	1	1	1
0.900	1	1	0	0	0
0.875	1	1	0	0	1
0.850	1	1	0	1	0
0.825	1	1	0	1	1
0.800	1	1	1	0	0
0.775	1	1	1	0	1

```
+VGPU_CORE
Countinue current:18A
Peak current:24A
OCP minimum 30A
Loadline=1.5mV/A
```

